What is claimed is:

1. A method of generating an integrated circuit netlist, comprising the steps of:

generating a first schematic of an integrated circuit having a plurality of cells therein;

generating a second schematic that defines post-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the post-layout interconnects; and

combining the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

2. The method of Claim 1, wherein said step of generating a second schematic comprises the steps of:

generating a layout schematic from the first schematic of the integrated circuit;

generating parasitic resistances and capacitances of the post-layout interconnects that extend between a plurality of cells in the layout schematic; and

generating parasitic resistances and capacitances of interconnects internal to at least one cell in the layout schematic.

3. The method of Claim 2, wherein said step of combining the first and second schematics comprises combining the first and second schematics into a simulation schematic.

4. The method of Claim 3, further comprising the steps of:

generating a netlist of at least a portion of the simulation schematic; and

supplementing the netlist with the parasitic resistances and capacitances of interconnects internal to the at least one cell in the layout schematic.

5. A computer program product that is configured to generate an integrated circuit netlist, comprising a computer-readable storage medium having computer-readable program code embodied in said medium, said computer-readable program code comprising:

computer-readable program code that is configured to generate a first schematic of an integrated circuit having a plurality of cells therein;

computer-readable program code that is configured to generate a second schematic that defines post-layout electrical interconnects between the plurality of cells of the integrated circuit and approximate parasitic resistances and parasitic capacitances of the post-layout interconnects; and

computer-readable program code that is configured to combine the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

6. The product of Claim 5, wherein said computer-readable program code that is configured to generate a second schematic comprises:

computer-readable program code that is configured to generate a layout schematic from the first schematic of the integrated circuit;

computer-readable program code that is configured to generate parasitic resistances and capacitances of the post-layout interconnects that extend between a plurality of cells in the layout schematic; and

computer-readable program code that is configured to generate parasitic resistances and capacitances of interconnects internal to at least one cell in the layout schematic.

7. The product of Claim 6, wherein said computer-readable program code that is configured to combine the first and second schematics comprise computer-readable program code that is configured to combine the first and second schematics into a simulation schematic.

8. The product of Claim 7, further comprising:

computer-readable program code that is configured to generate a netlist of at least a portion of the simulation schematic; and

computer-readable program code that is configured to supplement the netlist with the parasitic resistances and capacitances of interconnects internal to the at least one cell in the layout schematic.

9. A method of generating an integrated circuit netlist, comprising the steps of:

generating a first schematic of an integrated circuit having a plurality of cells therein;

generating a second schematic that defines pre-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the pre-layout interconnects; and

combining the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

10. An integrated circuit netlist generation apparatus, comprising:

means for generating a first schematic of an integrated circuit having a plurality of cells therein;

means for generating a second schematic that defines pre-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the pre-layout interconnects; and

means for combining the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

11. A selective netlist generation device for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the device comprising:

a schematic circuit generation unit for generating a schematic circuit in response to input information including information on circuit devices included in respective cells, information on connections between the circuit devices, and schematic layout information of the cells; and

a selective netlist output unit for selecting at least one cell included in the schematic circuit and generating a netlist of the selected cell, in response to selection information.

12. A selective netlist generation device for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the device comprising:

a selective netlist processor for generating a selective netlist of a schematic circuit including cells, a simulation schematic circuit obtained by combining the schematic circuit and an interconnection schematic circuit, and cells performing specific operations of the simulation schematic circuit, in response to input information including information on circuit devices included in the respective cells, information on connections between the circuit devices, and schematic layout information of the cells, information on interconnections interconnecting the cells, and selection information for selecting cells performing specific operations among the cells; and

an interconnection generator for generating interconnections in response to position information of cells included in the schematic circuit provided from the selective netlist processor and providing information on the generated interconnections to the selective netlist processor.

13. The device as claimed in claim 12, wherein the selective netlist processor comprises:

a schematic circuit generation unit for generating the schematic circuit in response to the input information;

an interconnection schematic circuit generation unit for generating a schematic circuit of the interconnections in response to the information on the interconnections;

a simulation schematic circuit generation unit for generating the simulation schematic circuit by combining first ports included in the cells of the schematic circuit and second ports of the interconnection schematic circuit corresponding to the first ports; and

a selective netlist output unit for selecting cells performing specific operations of the simulation schematic circuit and generating a selective netlist of the selected cells.

14. The device as claimed in claim 13, wherein the schematic circuit generated by the interconnection schematic circuit generating circuit maintains positional relations between the cells and includes a hybrid π model.

15. The device as claimed in claim 14, wherein non-selected cells connected to the cells selected by the selection information via the interconnections are used as capacitance devices.

16. A selective netlist generation device for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the device comprising:

a selective netlist processor for generating a selective netlist of a schematic circuit including cells, a simulation schematic circuit obtained by combining the schematic circuit and an interconnection schematic circuit, and cells performing specific operations of the simulation schematic circuit, in response to input information including information on circuit devices included in the respective cells, information on connections between the circuit devices, and schematic layout information of the cells, a netlist of parasitic resistance and parasitic capacitance, which are parasitic on the layout of the interconnections interconnecting the cells, and selection information for selecting cells performing specific operations among the cells;

a layout generator for generating a layout of the semiconductor integrated circuit in response to the information on the schematic circuit provided from the selective netlist processor; and

a parasitic RC extractor for extracting a netlist of the parasitic resistance and parasitic capacitance, which are parasitic on the layout of the interconnections, generated from the layout generator and providing the extracted netlist to the selective netlist processor.

17. The device as claimed in claim 16, wherein the selective netlist generation device combines the selective netlist of the parasitic resistance and parasitic capacitance, which are parasitic on the layout of the cells extracted by the parasitic RC extractor, with the selective netlist of the selected cells to generate a combined selective netlist.

18. The device as claimed in claim 17, wherein the selective netlist processor comprises

a schematic circuit generation unit for generating the schematic circuit in response to the input information;

an interconnection schematic circuit generation unit for generating the schematic circuit of the interconnections in response to the netlist of the parasitic resistance and parasitic capacitance;

a simulation schematic circuit generation unit for combining first ports included in the cells of the schematic circuit and second ports of the interconnection schematic circuit corresponding to the first ports to generate the simulation schematic circuit; and

a selective netlist output unit for selecting cells performing specific operations of the simulation schematic circuit and generating a selective netlist of the selected cells.

19. The device as claimed in claim 18, wherein the schematic circuit generated by the interconnection schematic circuit has a tree structure.

20. The device as claimed in claim 19, wherein non-selected cells connected to the cells selected by the selection information via the interconnections are used as capacitance devices.

21. A selective netlist generation device for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the device comprising:

a selective netlist processor for generating a selective netlist of a schematic circuit including cells, a first simulation schematic circuit obtained by combining the schematic circuit and an interconnection schematic circuit, a second simulation schematic circuit obtained by combining the schematic circuit and a schematic circuit corresponding to a netlist of parasitic resistance and parasitic capacitance, and cells performing specific operations of the simulation schematic circuit, in response to input information including information on circuit devices included in the respective cells, information on connections between the circuit devices, and schematic layout information of the cells, information the interconnections interconnecting the cells, and selection information for selecting cells performing specific operations among the cells;

an interconnection generator for generating the interconnections in response to positional information of the cells included in the schematic circuit provided from the selective netlist processor and providing the generated information on the interconnections;

a layout generator for generating a layout of the semiconductor integrated circuit in response to the information on the schematic circuit provided from the selective netlist processor; and

a parasitic RC extractor for extracting a netlist of the parasitic resistance and parasitic capacitance, which are parasitic on the layout of the interconnections, generated from the layout generator, and providing the extracted netlist to the selective netlist processor.

22. The device as claimed in claim 21, wherein the selective netlist generation device combines the selective netlist of the parasitic resistance and parasitic capacitance, which are parasitic on the layout of the cells extracted by the parasitic RC extractor and the selective netlist of the selected cells to generate a combined selective netlist.

23. The device as claimed in claim 22, wherein the selective netlist processor comprises:

a schematic circuit generation unit for generating the schematic circuit in response to the input information;

a first interconnection schematic circuit generation unit for generating the schematic circuit of the interconnections in response to the information on the interconnections;

a second interconnection schematic circuit generation unit for generating the schematic circuit of the interconnection layout in response to the netlist of the parasitic resistance and parasitic capacitance;

a simulation schematic circuit generation unit for combining first ports included in the cells of the schematic circuit and second ports of the interconnection schematic circuit corresponding to the first ports to generate and store the first simulation schematic circuit, and combining the first ports included in the cells of the schematic circuit and the second ports of the schematic circuit of the interconnection

layout corresponding to the first ports, wherein the stored first simulation schematic circuit is replaced by the generated second simulation schematic circuit; and

a selective netlist output unit for selecting cells performing specific operations of the replaced simulation schematic circuit and generating a selective netlist of the selected cells.

24. The device as claimed in claim 23, wherein the schematic circuit generated by the first interconnection schematic circuit generating circuit maintains positional relations between the cells and includes a hybrid π model.

25. The device as claimed in claim 24, wherein the schematic circuit generated by the second interconnection schematic circuit has a tree structure.

26. The device as claimed in claim 25, wherein non-selected cells connected to the cells selected by the selection information via the interconnections are used as capacitance devices.

27. A method for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the method comprising:

(a) generating a schematic circuit in response to input information including information on circuit devices included in respective cells, information on connections between the circuit devices, and schematic layout information of the cells; and

(b) selecting at least one cell included in the schematic circuit and generating a netlist of the selected cell, in response to selection information.

28. A method for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the method comprising:

(a) generating a schematic circuit in response to input information including information on circuit devices included in respective cells, information on connections between the circuit devices, and schematic layout information of the cells;

(b) generating interconnections interconnecting the cells in response to positional information of the cells included in the generated schematic circuit;

(c) generating an interconnection schematic circuit including parasitic resistance and parasitic capacitance, which are parasitic on the generated interconnections;

(d) combining first ports included in the cells of the generated schematic circuit with second ports of the interconnection schematic circuit, corresponding to the first ports, to generate a simulation schematic circuit; and

(e) selecting specific cells in response to selection information for selecting cells performing specific operations of the simulation schematic circuit and generating a selective netlist of the selected cells.

29. The method as claimed in claim 28, wherein the interconnection schematic circuit generated in step (c) maintains positional relations between the cells and includes a hybrid π model.

30. The method as claimed in claim 29, wherein non-selected cells connected to the cells selected by the selection information of step (e) via the interconnections are used as capacitance devices.

31. A method for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the method comprising:

(a) generating a schematic circuit in response to input information including information on circuit devices included in respective cells, information on connections between the circuit devices, and schematic layout information of the cells;

(b) generating a layout of the semiconductor integrated circuit in response to the information on the generated schematic circuit;

(c) extracting a netlist including parasitic resistance and parasitic capacitance, which are parasitic on the generated layout of interconnections;

(d) generating an interconnection schematic circuit including the parasitic resistance and parasitic capacitance, which are parasitic on the layout of the interconnections, in response to the extracted netlist;

(e) combining first ports included in cells of the generated schematic circuit with second ports of the interconnection schematic circuit, corresponding to the first ports, to generate a simulation schematic circuit; and

(f) selecting specific cells of the simulation schematic circuit in response to selection information for selecting cells performing specific operations of the generated simulation schematic circuit.

32. The method as claimed in claim 31, wherein in step (d), the generated interconnection schematic circuit has a tree structure.

33. The method as claimed in claim 32, wherein non-selected cells connected to the cells selected by the selection information of step (f) via the interconnections are used as capacitance devices.

34. A method for generating a selective netlist, which is required to simulate a specific part of a semiconductor integrated circuit, the method comprising:

(a) generating a schematic circuit in response to input information including information on circuit devices included in respective cells, information on connections between the circuit devices, and schematic layout information of the cells;

(b) generating interconnections interconnecting cells in response to positional information of the cells included in the generated schematic circuit;

(c) generating a first interconnection schematic circuit including parasitic resistance and parasitic capacitance, which are parasitic on the generated interconnections;

(d) combining first ports included in cells of the generated schematic circuit with second ports of the interconnection schematic circuit, corresponding to the first ports, to generate a first simulation schematic circuit;

(e) generating a layout of the semiconductor integrated circuit in response to the information on the generated schematic circuit;

(f) extracting a netlist of the parasitic resistance and parasitic capacitance, which are parasitic on the generated layout of the interconnections;

(g) generating a second interconnection schematic circuit including the parasitic resistance and parasitic capacitance, which are parasitic on the layout of the interconnections, in response to the extracted netlist;

(h) combining first ports included in the cells of the generated schematic circuit and second ports of the second interconnection schematic circuit,

corresponding to the first ports, to generate a second simulation schematic circuit and replace the stored first simulation schematic circuit by the second simulation schematic circuit; and

(i) selecting specific cells of the second simulation schematic circuit in response to selection information for selecting cells performing specific operations of the replaced second simulation schematic circuit and generating a selective netlist of the selected cells.

35. The method as claimed in claim 34, further comprising:

(j) extracting a netlist of parasitic resistance and parasitic capacitance, which are parasitic on the layout of the selected cells; and

(k) combining the selective netlist generated in step (i) with the netlist extracted in step (j) to generate a combined netlist.

36. The method as claimed in claim 35, wherein the first interconnection schematic circuit generated in step (c) maintains positional relations between the cells and includes a hybrid π model.

37. The method as claimed in claim 36, wherein the second interconnection circuit generated in step (g) has a tree structure.

38. The method as claimed in claim 37, wherein non-selected cells connected to the cells selected by the selection information of step (i) via the interconnections are used as capacitance devices.